REMARKS

This Amendment is submitted in response to the Office Action mailed June 14, 2005. Claims 1-4, 6, and 25-60 are presently pending. Claims 1-4, 6, and 25-60 stand rejected. By this amendment, claims 26, 30, 53, and 57 are amended. It is respectfully submitted that the pending claims define allowable subject matter.

Claims 1-4, 6, and 25-60 were rejected under 35 U.S.C. 112, first paragraph.

A. Claims 1-4, 6, 25, and 34-52.

Regarding claims 1-4, 6, 25, and 34-52, Examiner has indicated that:

> "In particular, Fig. 6 shows the implementation the device used to create the first clock frequency. The second clock frequency (C1) is input into feedback loop (block 601). However, the second clock frequency is generated at the output of an NCO (block 603), which is not a[ ]part of the feedback loop (block 601). There is no "looping" operation performed from the output of the NCO to the input of the feedback loop. Therefore, it would have been obvious to one skill[ed] in the art at the time the invention was made that the first clock frequency is not generated using a phase locked loop, rather the first clock frequency is generated using a feedback loop, half period calculator, and NCO, wherein the half-period calculator and NCO are separate from the feedback loop (the half period calculator and the NCO are not a[ ]part of the feedback loop)."

Office Action, at 3.

It is respectfully submitted that (1) the present application does enable one skilled in the art to make and use a "a phase locked loop for generating the first clock frequency using said second clock frequency"; and (2) Figure 6 enables one skilled in the art to make and use a "a phase locked loop for generating the first clock frequency using said second clock frequency".

> **(1) The present application does enable one skilled in the art to make and use a "demultiplexer comprising a phase locked loop for generating the first clock frequency using said second clock frequency".**

For example, Examiner's attention is called to Application, Figure 5. In Figure 5, it can be seen that the phase lock loop (Digital PLL) generates first clock frequency, e.g. clock frequency F1, using second clock frequency, e.g., clock frequency C1. Although Examiner makes specific reference to Figure 6, it is respectfully noted that Figure 6 is "a block diagram of one embodiment of the subsystems of PLL 52 illustrated in Fig. 5", in contrast to an exclusive embodiment. Application, Paragraph 41 (Emphasis Added). Therefore, even if Examiner's characterization of the embodiment described in Figure 6 were to be correct, the present application does teach one skilled in the art to make and use "a phase locked loop for generating the first clock frequency using said second clock frequency", at the least, from Figure 5.

(2) Figure 6 enables one skilled in the art to make and use a "a phase locked loop for generating the first clock frequency using said second clock frequency"

Examiner indicated that "second clock frequency (C1) is input into feedback loop (block 601). However, the second clock frequency is generated at the output of an NCO (block 603), which is not a[ ]part of the feedback loop (block 601)." Office Action, at 3.

Figure 6, NCO generates F1. From the above statement by Examiner, it is unclear whether Examiner is stating F1 is the second clock frequency, i.e., C1 and F1 are the same, or whether Examiner meant to say "...the first clock frequency is generated at the output of an NCO (block 603)." Clarification would be greatly appreciated. It is respectfully submitted that "One embodiment of the present invention uses an all-digital PLL to generated clock F1 [e.g., first clock frequency] from the clock C1 [e.g., second clock frequency]." Application, paragraph 43.

Additionally, a "second order feedback loop 601 determines the period, performing the operations illustrated in Figs. 7A and 7B." Id., at paragraph 42. "To determine the Period (i.e., generate the original clock frequency), the method

is initiated and the phase is compared to the horizontal width as illustrated by block 700 and diamond 702A." Id. at paragraph 44 (Emphasis Added).

Accordingly, it is respectfully submitted that Figure 6 teaches one skilled in the art to make and use a "a phase locked loop for generating the first clock frequency using said second clock frequency".

B. Claims 26-33 and 53-60

Claims 26-33 and 53-60 were also rejected under 35 U.S.C. 112, first paragraph. Claim 26 is amended to include, among other limitations, "a receiver comprising a demultiplexer, said receiver for acquiring said composite stream, and said demultiplexer comprising at least a second order feedback loop for determining a period of the first clock frequency." Claim 30 is amended to include "a receiver comprising a demultiplexer, said receiver for acquiring said composite stream, and said demultiplexer comprising at least a half period calculator circuit for generating at least one full cycle of the first clock frequency." Claims 53 and 57 are similarly amended. It is respectfully submitted that the rejection under 35 U.S.C. 112, first paragraph is overcome from the foregoing amendments.

C. Conclusion

For at least the foregoing reasons, all of the pending claims are allowable. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

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